REMARKS

Applicant has cancelled claim 2 and amended claim 1 to include the limitations of claim 2. Claim 3 has been amended to correct its dependency in light of the cancellation of claim 2.

Applicant thanks the Examiner for allowing claims 5-10.

Claims 1, 3 and 4 have been rejected under 35 USC 102(b) as anticipated by the Background of the Invention section of this application. Applicant has amended claim 1 to include the limitations of cancelled claim 2, so the rejection of claims 1, 3 and 4 under 35 USC 102(b) on the Background section of the application should be withdrawn.

Claims 1-4 have been rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 6,259,039 (Chroneos). Applicant respectfully disagrees.

The Examiner refers to Chroneos as U.S. Patent No. 6,805,279 in paragraph 2 of the Action. Applicant notes that this patent number is for Lee, which is relied upon by the Examiner in the rejection below, and Chroneos is indeed U.S. Patent 6,259,039, as properly cited in the Notice of References Cited.

Claim 1 as amended recites suspending by a plurality of pins the semiconductor wafer in a reflow furnace so that the metal portions are positioned upwardly in the reflow furnace. This amendment finds support, for example, at page 8, lines 16-20, of the specification. The Examiner contends that Chroneos's "circuit board" corresponds to the claimed semiconductor wafer. Applicant respectfully disagrees.

Chroneos does not refer to any structure by the expression "circuit board." Chroneos's circuit board carrier 102 is "produced using conventional printed circuit board (PCB) fabrication techniques and processes, and is generally made of FR4 laminate materials." See, column 2, lines 53-56, of Chroneos. Accordingly, a "printed circuit board" cannot be a semiconductor wafer as claimed. Thus, the Examiner must have meant to equate the claimed semiconductor wafer to Chroneos's surface mount assembly 202, which is mounted on the circuit board carrier 102 via solder balls 120 which the Examiner equates to the claimed metal portions. However, when Chroneos's device is subjected to the reflow process, the surface mount assembly 202 is

placed on the solder balls 202 that have been pre-fabricated on the circuit board carrier 102. Accordingly, Chroneos's solder balls 120 provided on the surface mount assembly 202 are positioned downwardly in Chroneos's reflow furnace and are not positioned upwardly as claimed.

The rejection of claims 1, 3 and 4 under 35 USC 102(b) on Chroneos should be withdrawn because Chroneos does not teach or suggest the claimed suspending of the semiconductor wafer in a reflow furnace so that the metal portions provided on the wafer are positioned upwardly in the reflow furnace.

Claims 1, 3 and 4 have been rejected under 35 USC 102(b) as anticipated by Lee. Applicant has amended claim 1 to include the limitations of cancelled claim 2, so the rejection of claims 1, 3 and 4 under 35 USC 102(b) on Lee should be withdrawn.

In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. 492322015200.

Respectfully submitted,

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